07-26-00

A

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	S1022/8500
First Named Inventor or Application Identifier	
CLAVERIE, Isabelle	
Express Mail Label No.	EL 018 096 242 US
Date of Deposit	July 25, 2000

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: **Box Patent Application**
Commissioner for Patents
Washington, DC 20231

1. ☐ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. [x] Specification [Total pages 11]
7 - pages description
1 - pages abstract
3 - pages claims 16 - Total claims

3. [x] Drawing(s) *(35 USC 113)* [Total sheets 3]
☐ Informal [x] Formal [Total drawings 1-6]

4. [x] Oath or Declaration [Total pages 3]
a. ☐ Newly executed (original or copy)
b. [x] Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. [x] Incorporation by Reference
(usable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Microfiche Computer Program (Appendix)

7. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers/cover sheet & documents(s)

9. ☐ 37 CFR 3.73(b) Statement
(when there is an assignee)
☐ Power of Attorney

10. ☐ English Translation of Document *(if applicable)*

11. [x] Information Disclosure Statement PTO-1449
[x] Copies of IDS Citations

12. ☐ Preliminary Amendment

13. [x] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)

14. ☐ Small Entity Statement(s)
☐ Statement filed in prior application, Status still proper and desired

15. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)

16. Other: PURSUANT TO 35 U.S.C. §119, APPLICANT HEREBY CLAIMS PRIORITY TO FRENCH PATENT APPLICATION 97/07741, FILED JUNE 17, 1997

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation [x] Divisional ☐ Continuation-in-part (CIP) of prior application No.: 09/094,341

☐ Cancel in this application original claims of the prior application before calculating the filing fee.

☐ Amend the specification by inserting before the first line the sentence:

18. CORRESPONDENCE ADDRESS					
Correspondence address below					
ATTORNEY'S NAME	James H. Morris, Reg. No. 34,681				
NAME	Wolf, Greenfield & Sacks, P.C.				
ADDRESS	600 Atlantic Avenue				
CITY	Boston	***STATE***	MA	***ZIP***	02210
COUNTRY	USA	***TELEPHONE***	(617) 720-3500	***FAX***	(617) 720-2441

19. SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED	
NAME	James H. Morris, Reg. No. 34,681
SIGNATURE	
DATE	July 25, 2000

PROTECTION OF THE LOGIC WELL OF A COMPONENT INCLUDING AN INTEGRATED MOS POWER TRANSISTOR

Cross Reference To Related Application

This application is a division of application serial number 09/094,341, filed June 9, 1998, entitled PROTECTION OF THE LOGIC WELL OF A COMPONENT INCLUDING AN INTEGRATED MOS POWER TRANSISTOR, which prior application is incorporated herein by reference.

Background Of The Invention

1. Field of the Invention

The present invention relates to components associating in the same substrate vertical diffused-type MOS power transistors (VDMOS) and logic circuits, and more specifically relates to the use of such components in circuits supplied by a battery, such as automobile circuits.

2. Discussion of the Related Art

Fig. 1 very schematically shows a portion of such a component. This component includes an N-type substrate generally formed of an N-type epitaxial layer 1 formed on an N^+-type substrate 2. A power transistor is formed in the right-hand portion and a logic well is formed in the left-hand portion.

The power transistor includes a set of identical cells connected to one another, such as cell 3. Each cell includes a P-type well 4, the central portion 5 of which is more heavily doped. An N-type ring 6 is formed in the upper portion of the well. The portion separating the external periphery of ring 6 from the external periphery of well 4 is coated with an isolated gate 8. N-type ring 6 as well as central portion 5 of the well are coated with a metallization 9. All gates 8 are connected to a gate terminal G and all metallizations 9 are connected to a source terminal S. The rear surface of the structure is coated with a drain metallization D. Thus, when a gate signal is applied, a current is likely to flow from terminal D to terminal S from N regions 1 and 2 to N regions 6, via a channel formed under the insulated gates. This structure is generally used so that the drain is biased to a positive potential with respect to the source.

Elements of logic circuits are formed in one or several wells 10. An elementary MOS transistor 11 having drain, source, and gate terminals g, d, and s has been shown in a well 10. This is only an example of a component that could be formed in a logic well.

The voltages on the several components formed in the logic well must be applied with respect to a reference. The simplest way to provide this reference, that is, to implement a ground connection, is illustrated in Fig. 1 and corresponds to the use of a well contacting area 12 formed on a region 13 of same type (P) as the well and more heavily doped. Contact 12 may be connected directly to the ground in simple embodiments. Generally, it should be understood that, for example, high voltages VDD are applied to some drains of the MOS transistors of the logic circuit which have their sources connected to contact 12 and to the ground.

Fig. 2 shows an example of an assembly of a component of the type shown in Fig. 1. The component is generally designated by block 20 surrounded with a frame in dotted lines. A reverse diode D1 is illustrated in parallel between the drain and the source of MOS power transistor T and corresponds to the junction between N-type substrate 1 and P-type region 5. Well 10 is represented by a block and it is assumed that it is connected to drain D of the MOS transistor via a diode D2 corresponding to the junction between substrate 1 and well 10.

In a very simple example of assembly, contact 12 of the well is grounded by a connection 21; and the source of the power transistor is connected to the ground via a load L, the switched supply of which is desired to be performed by the power transistor. A supply source such as a battery 23 is connected between the ground and drain terminal D of power transistor T. Thus, in normal operation, diodes D1 and D2 are reverse biased. According to its control, transistor T will be turned on or not and no current flows from the ground (contact 12) to the rear surface of the component (terminal D) due to the existence of reverse-biased diode D2.

Two incidents likely to occur in battery-powered circuits, and more specifically in automobile circuits, should however be considered.

The first incident corresponds to a biasing inversion of the battery. Diodes D1 and D2 are then forward biased. The current in diode D1 is limited by the presence of load L. Thus, the current will essentially flow through diode D2, as indicated by arrow 24. This current is likely to be destructive.

A second incident corresponds to a supply interruption, or battery disconnection, likely to occur when, due to vibrations or for any other reason, a lead wire of the battery breaks or operates intermittently. Then, if load L is inductive, the current will continue to flow therethrough according to the path designated by arrow 26. It should be noted that this current will necessarily exist, load L having to be considered as a current source. In the case of the simple assembly of Fig. 1, this current flow raises no specific problem. The problems result from the use of known protections against battery voltage inversions, as will be seen hereafter.

A first conventional solution to solve the battery inversion problem consists of inserting a diode, biased in a direction opposite to that of diode D2, in series with the well. The inserting of a diode may for example be performed in the way illustrated in Fig. 1, by adding an N^+-type region 15, grounding this region 15 by a connection 17, and suppressing the connection to ground 21. Various solutions have been provided to optimize the operation of this diode, and to have a well referenced to the ground when the circuit is in a normal operation state. Reference will especially be made to US patent no. 5099302 (Antoine Pavlin) relating to an active diode which is incorporated herein by reference. There still remains the problem that, in the case of a battery disconnection, current 26 will have to cross an avalanching diode and will dissipate a high power therein, which can cause a destruction of the component, unless a diode having a large surface is provided, which unduly increases the cost of the component.

A second conventional solution to the battery inversion problem consists of placing in series in connection 21 a resistor, a terminal of which will form the ground connection. But a new dilemma, difficult to solve, arises. Indeed, in normal operation, the resistance must be as low as possible to limit the voltage drop thereacross caused by the consumption of the elements of the logic circuit. Conversely, to solve the problems linked to the battery inversion case, this resistance must be as high as possible to limit the current flowing through the well.

Summary Of The Invention

Thus, an object of the present invention is to provide a structure for ground connection of the logic well of a component integrating a power transistor and logic elements which does not adversely affect the normal state operation, which prevents the current flow in the logic circuit in case of a battery inversion, and which lets through the current resulting from a battery disconnection.

To achieve these and other objects, the present invention provides a structure for ground connection on a component including a vertical MOS power transistor and logic components, the substrate of a first type of conductivity of the component corresponding to the drain of the MOS transistor and the logic components being formed in at least one well of the second type of conductivity and on the upper surface side of the substrate. This structure includes, in the logic well, a region of the first type of conductivity on which is formed a metallization, to implement, on the one hand, an ohmic contact, and on the other hand, a rectifying contact.

According to an embodiment of the present invention, the rectifying contact corresponds to a contact with regions of the second type of conductivity.

According to an embodiment of the present invention, the rectifying contact corresponds to a Schottky contact.

The foregoing objects, features and advantages of the present invention will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings.

Brief Description Of The Drawings

Fig. 1 shows a conventional structure of a component associating a vertical MOS transistor and logic circuits;

Fig. 2 shows an example of assembly of the component of Fig. 1 associated with a battery;

Fig. 3 shows a logic well ground connection structure according to the present invention;

Figs. 4A and 4B show equivalent diagrams associated with the ground connection structure according to the present invention;

Fig. 4C shows a current-voltage characteristic;

Fig. 5 shows a simplified cross-sectional view of an example of a ground connection structure according to the present invention; and

Fig. 6 shows an alternative of a ground connection structure according to the present invention.

Detailed Description

In the various drawings, same elements are referred to with same references. Further, in the various cross-sectional views of semiconductor components, as is usual, the various dimensions are not drawn to scale but are arbitrarily expanded to facilitate the readability of the drawings.

The ground connection structure according to the present invention includes an N-type region 30 formed in logic well 10. Alternate N^+ and P^+-type regions, respectively designated by references 31 and 32 are formed in this N-type region, for example, in the form of a grid. Regions 31 and 32 are altogether coated with a metallization 33, itself normally connected to the circuit ground by a connection corresponding to connection 21 of Fig. 2.

Figs. 4A and 4B show two forms of an equivalent diagram of the ground connection structure, seen between connection 21 and terminal D (rear surface of the component). It can be considered that this structure corresponds to a thyristor Th, the anode of which corresponds to metallization 33 and the cathode of which corresponds to rear surface metallization D. The thyristor anode will correspond to P^+-type regions 32, and a resistive region will be located between the anode and the anode gate of this transistor, this resistor being referred to by reference r_{be}. Fig. 4B shows the same diagram, but in which the thyristor has been shown conventionally in the form of its equivalent transistors. P^+-type region 32, N well 30, and P-type well region 10 form a PNP transistor T1, the emitter of which is connected to metallization 33 and the base of which is connected via resistor r_{be} to metallization 33. Region 30, well 10, and substrate 1 form an NPN transistor T2, the emitter of which is connected to drain metallization D, the collector of which is connected to the base of transistor T1, and the base of which is connected to the collector of transistor T1. It should be noted that the common base region of transistor T2 and collector region of transistor T1 corresponds to well 10, that is, to reference potential VSS of the elements of the logic circuit formed in well 10.

Thus, during normal circuit operation, thyristor Th is reverse biased and no current can flow through the junction between substrate 1 and well 10.

The current-voltage characteristic of the structure appears in Fig. 4C in which a voltage V on metallization 33 is assumed to be positive with respect to terminal D which is then grounded, which occurs in case of a battery inversion. The junction between N well 30 and P well 10 is reverse biased and no current can flow as long as the applied voltage is lower than

breakdown voltage V_{BR} of this junction. The structure must be implemented so that voltage V_{BR} is higher than the reverse battery voltage, to protect the logic portion of the circuit formed in well 10.

In case of a battery disconnection, inductive load L causes a current to flow which forces the junction between N well 30 and P well 10 to start an avalanche. When the current flowing through resistor r_{be} reaches a threshold value, noted I_BR on Fig. 4C, such that the value of the voltage drop across the resistor is higher than 0.6 V, transistor T1 turns on. This supplies the base of transistor T2, which also turns on. In other words, this causes the break-over of thyristor Th and the voltage drop across this thyristor becomes very low, which allows dissipation of high currents without any risk of destruction in case of a battery disconnection under an inductive load. Break-over threshold I_BR must be optimized so that it is high enough not to cause any untimely break-over of the characteristic in case of battery inversion, and low enough for the structure to be able to dissipate current I_BR under breakdown voltage V_{BR}.

It should be noted, according to a first advantage of the present invention, that the triggering threshold of the protection circuit according to the present invention is easily adjustable. Indeed, considering a top view of this protection structure, such as shown in Fig. 5, P-type regions 32 can be considered as a grid separated by N-type regions 31. The surface ratio between P and N regions 32 and 31 determines the value of resistance r_{be}. The surface ratio between the P and N regions will for example be on the order of 15 to 1, the triggering current being lower when this ratio is higher. In an example of embodiment, each of squares 32 can have a side on the order of 8 μm and the distance between two squares can be 2 μm.

According to another advantage of the present invention, metallization 33 does not have a larger surface than the surface normally provided to establish a contact pad on P well 10. Thus, there is no surface increase with respect to the normal implementation of the well. It will again be stressed that the representations of the various drawings are not to scale.

The operating modes in battery inversion and disconnection states have been described hereabove. The logic well also has to be at the ground potential in normal operation. For this purpose, a structure such as illustrated in Fig. 3 may for example be used, taking inspiration from the structure described in above-mentioned US patent no. 5099302. For example, a heavily-doped P-type region 35 connected to the ground via a MOS transistor 37 is provided. The gate of transistor 37 is connected to terminal D, whereby MOS transistor 37 is on when the

battery is properly connected (normal operation) and off in all other cases (battery inversion or disconnection state).

Fig. 6 shows an alternative of the circuit according to the present invention in which the same elements as in Fig. 3 appear, designated by the same references. The difference between the two drains is that P^+-type regions 32 have been suppressed and the doping level of N-type region 30 is chosen to form a Schottky diode with metallization 33, which will for example be made of aluminum. The Schottky diode causes a limited injection of minority carriers, which is less efficient than P^+-N junction 32-30, but sufficient to create a bipolar effect similar to that created by transistor T1 of Fig. 4B. This structure has the advantage of eliminating one P^+ masking level.

Of course, the present invention is likely to have various alterations, modifications, and improvements which will readily occur to those skilled in the art. Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:

CLAIMS

1. A circuit, comprising:

an input to receive a supply voltage, the supply voltage having a normal polarity and an inverted polarity;

an output to drive a load, the load being connected between the output and a ground;

a logic component, connected between the input and the output, to electrically couple the load to the supply voltage when the supply voltage has the normal polarity; and

a protection component, connected between the input and the ground, to prevent a first current from flowing in the circuit when the supply voltage has the inverted polarity, and to allow a second current to flow in the circuit if the supply voltage is disconnected from the input.

2. The circuit of claim 1, wherein the protection component prevents the first current from flowing between the supply voltage and the ground when the supply voltage has the inverted polarity.

3. The circuit of claim 1, wherein:

the load is an inductive load; and

the second current flows between the load and the ground through the protection component when the supply voltage is disconnected.

4. The circuit of claim 1, wherein the protection component is a thyristor.

5. The circuit of claim 4, wherein the thyristor is reverse biased when the supply voltage has the normal polarity.

6. The circuit of claim 4, wherein the thyristor is forward biased but not conducting when the supply voltage has the inverted polarity.

7. The circuit of claim 4, wherein:

the thyristor has a forward breakdown voltage; and

the forward breakdown voltage is greater than the supply voltage having the inverted polarity.

8. The circuit of claim 4, wherein the protective component further includes a resistor connected between the ground and the thyristor.

9. The circuit of claim 8, wherein a break-over current flowing through the resistor causes the second current to flow through the thyristor.

10. The circuit of claim 9, wherein the break-over current is adjustable.

11. The circuit of claim 10, wherein:
the thyristor has a breakdown voltage; and
the breakdown voltage is greater than the supply voltage having the inverted polarity.

12. The circuit of claim 11, wherein the break-over current is adjusted based on the breakdown voltage.

13. A method of protecting a circuit which electrically couples a supply voltage to a load, comprising steps of:

preventing a first current to flow in the circuit between the supply voltage and the load when the supply voltage has an inverted polarity; and

allowing a second current to flow in the circuit between the load and a ground if the supply voltage is disconnected from the circuit.

14. The method of claim 13, wherein the step of preventing a first current to flow includes a step of preventing a first current to flow in the circuit between the supply voltage and the ground when the supply voltage has an inverted polarity.

15. The method of claim 13, wherein the step of preventing a first current to flow includes a step of selecting a breakdown voltage for a protection component in the circuit, the breakdown voltage being greater than the supply voltage having the inverted polarity.

16. The method of claim 14, wherein the step of allowing a second current to flow includes a step of selecting a trigger current for the protection component based on the breakdown voltage.

ABSTRACT

The present invention relates to a structure for ground connection on a component including a vertical MOS power transistor and logic components, the substrate of a first type of conductivity of the component corresponding to the drain of the MOS transistor and the logic components being formed in at least one well of the second type of conductivity and on the upper surface side of the substrate. In the logic well, a region of the first type of conductivity is formed, on which is formed a metallization, to implement, on the one hand, an ohmic contact, and on the other hand, a rectifying contact.

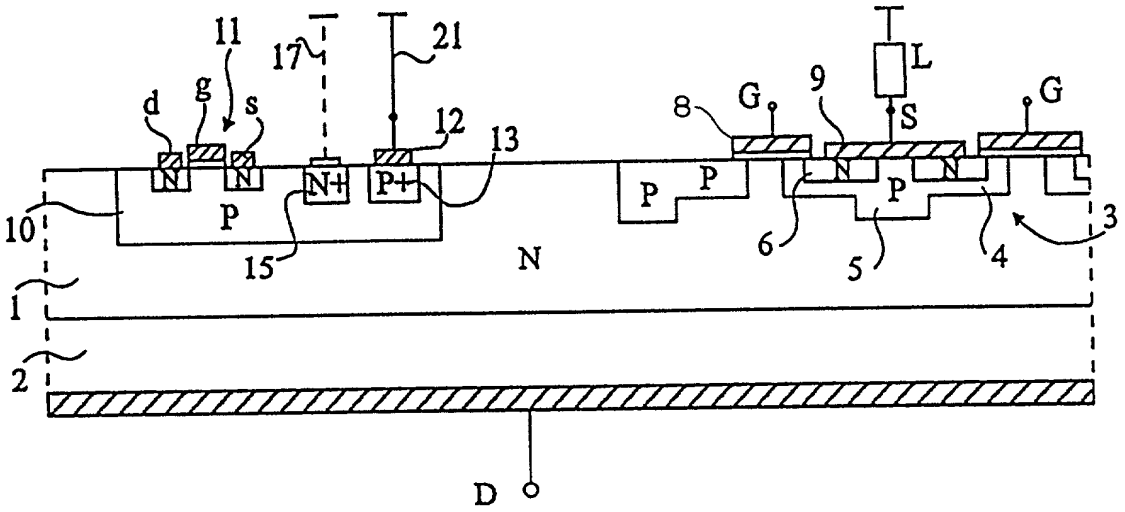

FIG. 1
(PRIOR ART)

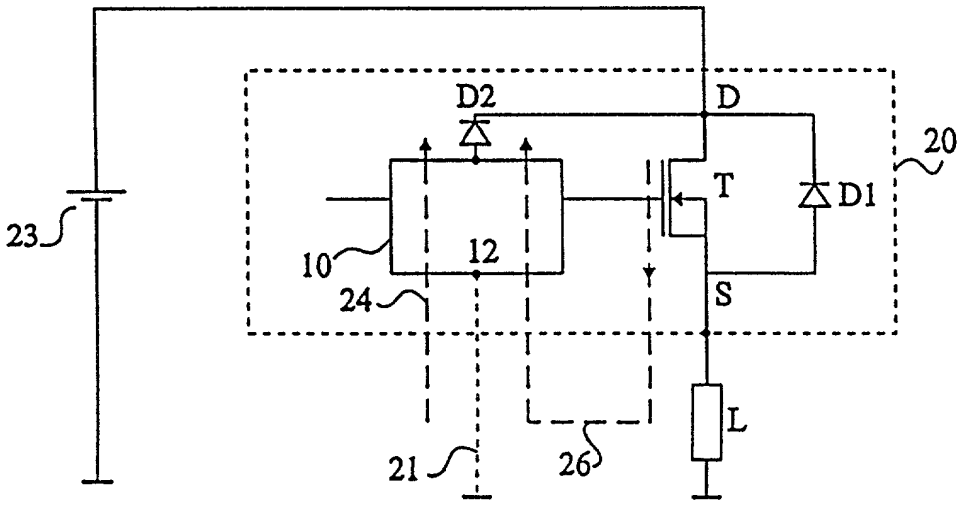

FIG. 2
(PRIOR ART)

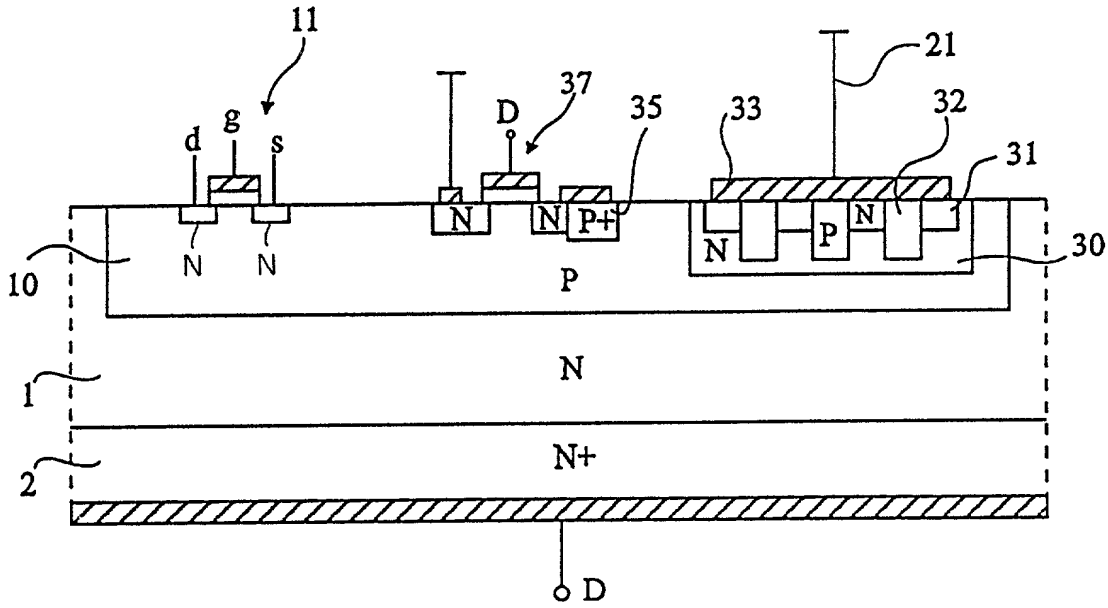

FIG. 3

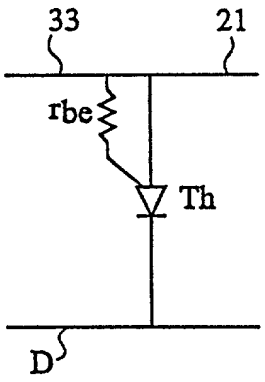

FIG. 4A

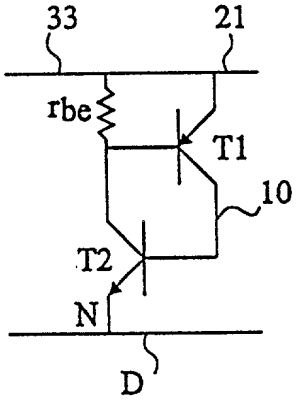

FIG. 4B

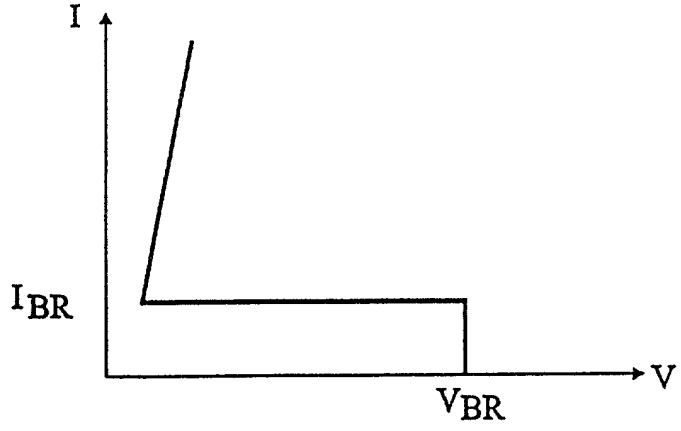

FIG. 4C

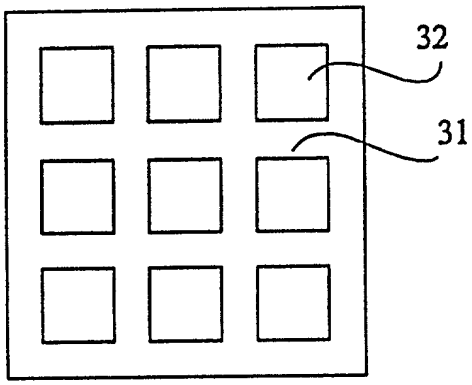

FIG. 5

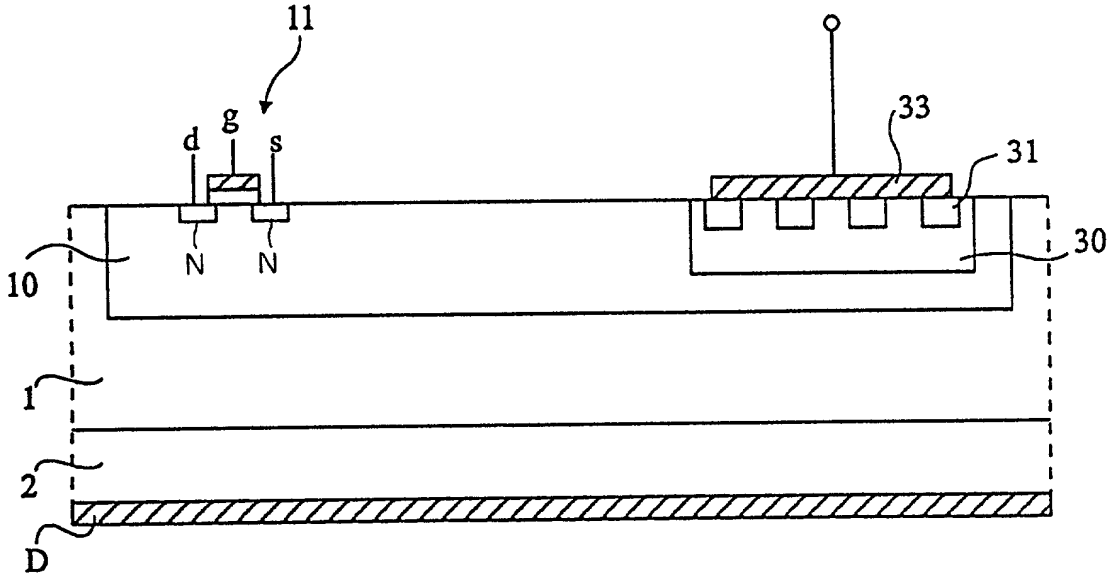

FIG. 6

Declaration and Power of Attorney for Patent Application

Déclaration et Pouvoirs pour Demande de Brevet

French Language Declaration

En tant que l'inventeur nommé ci-après, je déclare par le présent acte que:

As a below named inventor, I hereby declare that:

Mon domicile, mon adresse postale, et ma nationalité sont ceux figurant ci-dessous à côté de mon nom.

My residence, post office address and citizenship are as stated next to my name.

Je crois être le premier inventeur original et unique (si un seul nom est mentionné ci-dessous), ou l'un des premiers co-inventeurs originaux (si plusieurs noms sont mentionnés ci-dessous) de l'objet revendiqué, pour lequel une demande de brevet a été déposée concernant l'invention intitulée:

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PROTECTION OF THE LOGIC WELL OF A COMPONENT INCLUDING AN INTEGRATED MOS POWER TRANSISTOR

et dont la description est fournie ci-joint à moins que la case suivante n'ait été cochée:

the specification of which is attached hereto unless the following box is checked:

☒ a été déposée le 9 JUIN 1998 sous le numéro de demande des Etats-Unis ou le numéro de demande international PCT 09/094,341 et modifiée le _____ (le cas échéant).

☒ was filed on JUNE 9, 1998 as United States Application Number or PCT International Application Number 09/094,341 and was amended on _____ (if applicable).

Je déclare par le présent acte avoir passé en revue et compris le contenu de la description ci-dessus, revendications comprises, telles que modifiées par toute modification dont il aura été fait référence ci-dessus.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

Je reconnais devoir divulguer toute information pertinente à la brevetabilité, comme défini dans le Titre 37, §1.56 du Code fédéral des réglementations.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

PTO/SB/105(Rev. 5-95) OMB 0651-0032

French Language Declaration

Je revendique par le présent acte avoir la priorité étrangère, en vertu du Titre 35, §119(a)-(d) ou § 365(b) du Code des Etats-Unis, sur toute demande étrangère de brevet ou certificat d'inventeur ou, en vertu du Titre 35, § 365(a) du même Code, sur toute demande internationale PCT désignant au moins un pays autre que les Etats-Unis et figurant ci-dessous et, en cochant la case, j'ai aussi indiqué ci-dessous toute demande étrangère de brevet, tout certificat d'inventeur ou toute demande internationale PCT ayant une date de dépôt précédant celle de la demande à propos de laquelle une priorité est revendiquée.

I hereby claim foreign priority under Title 35, United States Code, §119(a)-(d) or § 365(b) of any foreign applications(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below, and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Prior foreign application(s) Demande(s) de brevet antérieure(s)		Priority not claimed Droit de priorité non revendiqué
97/07741 (Number) (Numéro)	FRANCE (Country) (Pays)	17 JUNE 1997 (Day/Month/Year Filed) (Jour/Mois/Année de dépôt) ☐
(Number) (Numéro)	(Country) (Pays)	(Day/Month/Year Filed) (Jour/Mois/Année de dépôt) ☐

Je revendique par le présent acte tout bénéfice, en vertu du Titre 35 §119(e) du Code des Etats-Unis, de toute demande de brevet provisoire effectuée aux Etats-Unis et figurant ci-dessous.

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

(Application No.) (N° de demande)	(Filing Date) (Date de dépôt)
(Application No.) (N° de demande)	(Filing Date) (Date de dépôt)

Je revendique par le présent acte, le bénéfice, en vertu du Titre 35 § 120 du Code des Etats-Unis, de toute demande de brevet effectuée aux Etats-Unis, ou en vertu du Titre 35, §365(c) du même Code, de toute demande internationale PCT désignant les Etats-Unis et figurant ci-dessous et, dans la mesure où l'objet de chacune des revendications de cette demande de brevet n'est pas divulgué dans la demande antérieure américaine ou internationale PCT, en vertu des dispositions du premier paragraphe du Titre 35, § 112 du Code des Etats-Unis, je reconnais devoir divulguer toute information pertinente à la brevetabilité, comme défini dans le Titre 37, § 1.56 du Code Fédéral des réglementations, dont j'ai pu disposer entre la date de dépôt de la demande antérieure et la date de dépôt de la demande nationale ou internationale PCT de la présente demande:

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or § 365(c) of any PCT international application(s) designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application No.) (N° de Demande)	(Filing Date) (Date de Dépôt)	(Status)(Patented, pending abandoned) (Statut)(breveté, en cours d'examen, abandonné)
(Application No.) (N° de Demande)	(Filing Date) (Date de Dépôt)	(Status)(Patented, pending abandoned) (Statut)(breveté, en cours d'examen, abandonné)

Je déclare par le présent acte que toute déclaration ci-incluse est, à ma connaissance, véridique et que toute déclaration formulée à partir de renseignements ou de suppositions est tenue pour véridique; et de plus, que toutes ces déclarations ont été formulées en sachant que toute fausse déclaration volontaire ou son équivalent est passible d'une amende ou d'une incarcération, ou des deux, en vertu de la Section 1001 du Titre 18 du Code des Etats-Unis, et que de telles déclarations volontairement fausses risquent de compromettre la validité de la demande de brevet ou du brevet délivré à partir de celle-ci.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

French Language Declaration

POUVOIR: En tant que l'inventeur cité, je désigne par la présente l'(les) avocat(s) et/ou agent(s) suivant(s) pour qu''il(s) poursuive(nt) la procédure de cette demande de brevet et traite(nt) toute affaire s'y rapportant avec l'Office des brevets et des marques: *(mentionner le nom et le numéro d'enregistrement).*

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

David Wolf	17,528	James J. Foster	30,052	John N. Anastasi	37,765	Lindsay G. McGuinness	38,549
George L. Greenfield	17,756	Charles E. Pfund	17,030	Helen C. Kindregan	39,248	Mike W. Crosby	40,970
Stanley Sacks	19,900	Jason M. Honeyman	31,624	James M. Hanifin, Jr.	39,213	Ivan D. Zitkovsky	37,482
Edward F. Perlman	28,105	James H. Morris	34,681	Christopher S. Schultz	37,929	Robert M. Abrahamsen	40,886
Lawrence M. Green	29,384	Peter C. Lando	34,654	Paul D. Sorkin	39,039	Michele J. Young	P-43299
Steven J. Henry	27,900	Gary S. Engelson	35,128	John R. VanAmsterdam	40,212	Alan B. Sherr	P-42147
Edward R. Gates	31,616	Peter J. Gordon	35,164	Matthew B. Lowrie	33,228	Edward J. Russavage	P-43069
Therese A. Hendricks	30,389	Randy J. Pritzker	35,986	Michael G. Verga	39,410	Theodore E. Galanthay	24,122
William R. McClellan	29,409	Richard F. Giunta	36,149	Robert E. Rigby, Jr.	36,904	Lisa K. Jorgenson	34,845
Ronald J. Krandsdorf	20,004	Douglas R. Wolf	36,971	Robert A. Skrivanek, Jr.	41,316	Mark E. McBurney	33,114
M. Lawrence Oliverio	30,915	Elizabeth R. Plumer	36,637	Robert M. Abrahamsen	40,886	Robert D. McCutcheon	38,717
		Timothy J. Oyer	36,628	Lesley A. Hamlin	41,054		

Adresser toute correspondance à:

Send correspondence to:
James H. Morris
Wolf, Greenfield & Sacks, P.C,
Federal Reserve Plaza
600 Atlantic Avenue, Boston, MA 02210-2211(USA)

Adresser tout appel téléphonique à:
(Nom et numéro de téléphone)

Direct Telephone Calls to: (name and telephone number)
James H. Morris
(617) 720-3500

Nom complet de l'unique ou premier inventeur Isabelle CLAVERIE	Full name of sole or first inventor
Signature de l'inventeur ~~Steven~~ CLAVERIE Isabelle Date 07/09/98	Inventor's signature Date
Domicile MARSEILLE, FRANCE	Residence
Nationalité French	Citizenship
Adresse Postale 13 Tr. Notre Dame de Bon Secours	Post Office Address
13003 MARSEILLE, FRANCE	
Nom complet du second co-inventeur, le cas échéant	Full name of second or joint inventor
Signature de l'inventeur Date	Inventor's signature Date
Domicile	Residence
Nationalité	Citizenship
Adresse Postale	Post Office Address

(Fournir les mêmes renseignements et la signature de tout co-inventeur supplémentaire.)

(Supply similar information and signature for third and sub-sequent joint inventors.)